IN THE SPECIFICATION

In the paragraph at page 13, lines 5 – 22, please correct as indicated:

Figure 3 is a functional block diagram of a microsequencer formed according to one embodiment of the present invention. A microsequencer 300 includes a 32-bit microcode read-only memory 304 that is for storing microcode (computer instructions that define the operational logic of the microsequencer of ~~Figure 3~~ Figure 3). Microcode read-only memory 304 further is coupled to receive control signals from a program counter (PC) 308 that further communicates with a stack 312. The control commands from PC 308 select what instruction(s) is(are) sent to a control decode module 316. Control decode module 316 is coupled to receive computer instructions produced by microcode read-only memory 304 and to execute the received instructions in accordance with the logic defined within microcode memory 304. Control decode module 316 further generates control commands to PC 308 to prompt it to change its program counter value (and therefore what instructions are sent from microcode ROM 304 to control decode ~~module 316~~ module 316).

In the paragraph at page 17, lines 11 - 26 through page 18, lines 1 - 4, please correct as indicated:

In order to satisfy Bluetooth requirements, the possibility exists that more than one real-time or Bluetooth clock is required. Because the inventor herein has realized that it is advantageous to create separate and independent clocks to maintain flexibility, among other benefits, a second set of clocks, namely the externally driven real-time clock 428 and the externally driven Bluetooth clock 424 are included. Each of these two clocks, however, is driven by a received clock signal from an external clock source 436 (for example, from an external master while the device in which circuitry 400 is installed is operating ~~as a slave~~ as a slave). As is known by those skilled in the art, when a device acts a slave, the timing of operations are determined by an external master. Accordingly, the present invention facilitates receiving clock signals from an external master for synchronizing the externally driven real time clock 428 to clock signals received from the external master. The synchronized and externally driven real time clock 428 then drives

a Bluetooth clock 424 to cause it to be synchronized with the external master's Bluetooth clock.

In the paragraph at page 20, lines 25-26 through page 21, lines 1-5, please correct as indicated:

Microsequencer 504 also is coupled to CRC FEC ~~Whiten encryption~~ Whitten encryption modules 536 and 572 that are for providing CRC error detection, error correction ~~and "whitening"~~ and "whittening" of a given stream of digital signals. The outputs of modules 536 and 572 are coupled to logic gates (exclusive OR in the described embodiment) which combines their outputs with data being output from or input to microsequencer 504.